Claims

1. A programmable logic device comprising an array of programmable logical elements, said programmable logic device characterized in that said logical elements include:

first logical elements having a predetermined logic; and

second logical elements having the same logic as said first logical elements but having an upper limit of operating speed designed to be lower than that of said first logical elements.

2. The programmable logic device according to Claim 1, wherein each of said second logical elements uses transistors higher in threshold voltage compared with transistors used in each of said first logical elements.

3. The programmable logic device according to Claim 1, wherein said second logical elements have a layout structure different from that of said first logical elements.

4. The programmable logic device according to any one of Claims 1 through 3, wherein the first logical elements are operated by a clock signal with a first clock frequency; and

said second logical elements are operated by a clock signal with a second clock frequency lower than said first clock frequency.

5. The programmable logic device according to any one of Claims

1 through 4, wherein said first logical elements are arranged collectively in one place.

6. The programmable logic device according to Claim 5, wherein said first logical elements are arranged in a center portion of said programmable logic device; and

said second logical elements are arranged in a peripheral portion of said programmable logic device with respective to the region where said first logical elements are arranged.

7. The programmable logic device according to Claim 5, wherein:

said second logical elements are arranged in a center portion of said programmable logic device; and

said first logical elements are arranged in a peripheral portion of said programmable logic device with respective to the region where said second logical elements are arranged.

8. A method of designing a programmable logic device formed from an array of programmable logical elements, said method characterized by comprising the steps of:

designing first logical elements having a predetermined logic; and

designing second logical elements having the same logic as said first logical elements but having an upper limit of operating speed designed to be lower than that of said first logical elements.